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14EVE23

Second Semester M.Tech. Degree Examination, June/July 2015
VLSI Testing and Verification

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions.*

1 a. Discuss about VLSI technology trends which affect testing. **(10 Marks)**
b. Explain the role of testing. **(04 Marks)**
c. Differentiate between analog testing and digital testing. **(06 Marks)**

2 a. Briefly explain about automatic test pattern generator [ATPG]. Mention and explain types of ATPG algorithms. **(12 Marks)**
b. Differentiate between controllability and observability. **(08 Marks)**

3 a. Explain boundary scan along with TAP architecture. **(10 Marks)**
b. Describe BIST technique used in design for test. **(10 Marks)**

4 a. Define testbench. Explain the importance of verification. Mention 3 ways to reduce verification time **(10 Marks)**
b. Differentiate between equivalence checking and model checking. **(10 Marks)**

5 a. Briefly explain linting tools with examples. What are the limitations of linting tools? **(10 Marks)**
b. Differentiate between cycle based simulation and event based simulation mention their merits and demerits. **(10 Marks)**

6 a. Define first time success. Explain role of verification plan. **(06 Marks)**
b. With neat block diagram explain the levels of verification. **(10 Marks)**
c. Write short notes on random verification. **(04 Marks)**

7 a. Define and explain static timing scaling. List and explain the limitations. **(12 Marks)**
b. Explain the following terms with example:
i) Skew between signals
ii) Timing arcs and tightness. **(08 Marks)**

8 a. Define crosstalk. Explain crosstalk delay analysis. **(08 Marks)**
b. What are design checks? Explain electrical and layout rule checks. **(05 Marks)**
c. Explain parasitic extraction and the methodologies for parasitic extraction. **(07 Marks)**

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